

Accelerating Memory-Access-Limited HPC Applications via Novel Fast Data Compression, Phase I

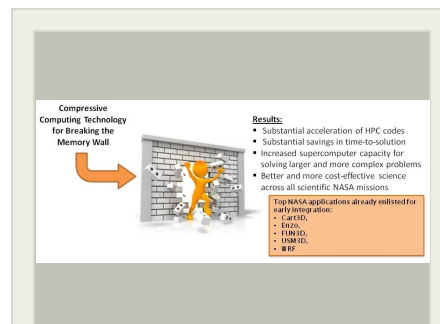
Completed Technology Project (2015 - 2015)



Project Introduction

A fast-paced continual increase on the ratio of CPU to memory speed feeds an exponentially growing limitation for extracting performance from HPC systems. Ongoing developments and trends make it clear that this ratio will keep increasing over the next decade. Breaking this memory wall is one of the most important challenges that the HPC community faces today. In this project we introduce novel and highly effective ways of attacking the memory wall through the use of "compressive computing," a theory that we have invented, developed, and successfully put into practice in other areas of HPC with paradigm-shifting results. Once integrated into memory-bound HPC applications, the proposed technology will support significant acceleration factors (typically beyond 2x) without compromising the numerical accuracy of the application code. In Phase I we will develop the fundamentals of the theory of compressive computing for memory access acceleration, deploy a set of functional components, and produce a fully functional prototype that demonstrates convincingly that the technology works for acceleration of memory-bound applications. The prototype will be integrated in at least one NAS Parallel Benchmark. In Phase II we will focus our work on maturing and refining the technology, and will be driven by a concrete target of accelerating at least two memory-access-bound NASA applications. Five of the top eight most-used application codes in NASA supercomputers have already signed-in as early integrators of the technology. We have secured complementary funds in the amount of \$150,000 that we will be able to use to increase resources and ensure that all Phase I proposed work will be successfully accomplished in a timely manner, and a total of \$500,000 to ensure a successful and early penetration of the proposed technology into the market.

Primary U.S. Work Locations and Key Partners



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Organizations Performing Work	Role	Type	Location
Accelelogic, LLC	Lead Organization	Industry	Weston, Florida
● Ames Research Center(ARC)	Supporting Organization	NASA Center	Moffett Field, California

Primary U.S. Work Locations

California	Florida
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Project Transitions

▶ **June 2015:** Project Start

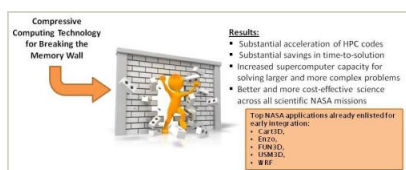
✓ **December 2015:** Closed out

Closeout Summary: Accelerating Memory-Access-Limited HPC Applications via Novel Fast Data Compression, Phase I Project Image

Closeout Documentation:

- Final Summary Chart Image(<https://techport.nasa.gov/file/138649>)

Images

**Briefing Chart Image**

Accelerating Memory-Access-Limited HPC Applications via Novel Fast Data Compression, Phase I
(<https://techport.nasa.gov/image/128132>)

Organizational Responsibility

Responsible Mission Directorate:

Space Technology Mission Directorate (STMD)

Lead Organization:

Accelelogic, LLC

Responsible Program:

Small Business Innovation Research/Small Business Tech Transfer

Project Management

Program Director:

Jason L Kessler

Program Manager:

Carlos Torrez

Principal Investigator:

Juan Gonzalez

Co-Investigator:

Juan Gonzalez

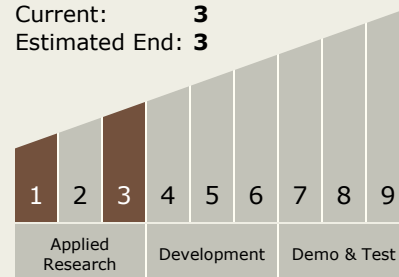
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Technology Maturity (TRL)

Start: **1**
Current: **3**
Estimated End: **3**



Technology Areas

Primary:

- TX11 Software, Modeling, Simulation, and Information Processing
 - └ TX11.6 Ground Computing
 - └ TX11.6.2 Automated Exascale Software Development Toolset

Target Destinations

The Moon, Mars, Outside the Solar System, The Sun, Earth, Others Inside the Solar System